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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,399	03/31/2000	Youfeng Wu	884.217US1	3990

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EXAMINER
WOOD, WILLIAM H

ART UNIT	PAPER NUMBER
2124	11

DATE MAILED: 09/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/541,399	WU ET AL.	
	Examiner	Art Unit	
	William H. Wood	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) *1-12 and 26-39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,15-22,24,25 and 40-67* is/are rejected.

7)☐ Claim(s) *14 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 13-25 and 40-67 have been examined.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 July 2003 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 50-67 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 50 contains the limitation *selecting a CFG of a program for profiling*. This limitation is not enabled by the specification as one would not now how to "select" a CFG, there would be just one CFG of the program from which to start the claimed method.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 49 and 67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 49 and 67 are apparatus claims dependent on method claims 40 and 50 respectively. Such a relationship constitutes an improper dependency and renders the claims 49 and 67 unclear as to whether it is a method claim or an apparatus claim. The claims 49 and 67 should be rewritten in an independent form.

6. Claims 40-67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 40 and 50 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: one or more steps explaining how *assigning identifiers to the edges* can result in *producing a unique combination of the identifiers.*

7. Claims 40-67 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: *replacing the inner region with a representative node.*

8. Claims 50-67 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 50 contains the limitation *inserting additional edges into the CFG to produce an augmented CFG, at least some of the edges extending between an outer one of the regions and an inner one of the regions*. The difference between the outer one and the inner one of the regions is unclear from the claim language. Appropriated correction is required. Claims 51-67 are rejected as being dependent on claim 50.

9. Claims 64-66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 64 contains the limitation *{p19:29}* in the second line of the claim. This confuses the clarity of the claim and must be removed. Claims 65-66 are dependent on rejected claim 64.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 13, 18-22 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Breternitz, Jr.** et al. (USPN 6,381,739) in view of **Tenev** et al. (USPN 6,108,698) in further view of **Bharadwaj** (USPN 5,894,576).

In regard to claim 13, **Breternitz, Jr.** disclosed the limitations:

- *A computer-implemented method* (title; column 1, lines 19-22) *comprising:*
  - *providing a control flow graph of a program, the graph having an inner region with entry node, and an outer region* (column 13, lines 32-54; column 14, liens 5-35; Figures 14-20);

Breternitz, Jr. did not explicitly state *selecting a single one of the existing entry nodes as a representative entry node for the inner region* and *replacing the inner region with the representative entry node*. **Tenev** demonstrated that it was known at the time of invention to construct graphs such that one node is selected as a representative of other nodes (Figure 9; element 510 and 514) and replacing the other nodes with the single node (Figure 9, elements 520, 522 and 524). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Breternitz, Jr.**'s single entry single exit control flow graph system with one selected node as representative of other nodes as found in **Tenev**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide more information in a single graph (for example, this aids in expansion and contraction of nodes, column 3, liens 25-34); additionally, along this same line of reasoning, the implementation would have been obvious because of ordinary skill in the art would be

motivated to provide the compiler optimizations to a greater amount of code, which would be represented with a compact CFG containing global information.

Neither **Breternitz, Jr.** nor **Tenev** did not explicitly state *inner region with multiple entry nodes; for each prolog node of the inner region having an edge to one of the existing entry nodes other than the representative entry node, adding an edge from the prolog node to the representative entry node; and for each epilog node of the inner region, adding an edge from the representative entry node to the epilog node*. **Bharadwaj** demonstrated that it was known at the time of invention to provide control flow regions with multiple entry and exit ,oints (column 4, line 61 to column 5, line 14), which implies multiple prolog nodes with an edge other than the "representative" entry node and epilog nodes as well (remembering super/extended basic blocks have multiple exits to other nodes and reverse super/extended basic blocks have multiple entries from other nodes). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the single entry single exit CFG of **Breternitz, Jr** and **Tenev** with CFG's having multiple entry nodes and with adding an edge between entry and prolog/epilog nodes as suggested by **Bharadwaj**'s teaching and **Tenev**'s use of a single node. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implementing standard CFG situations (multiple prolog nodes) with the benefits of single entry single exit (**Breternitz, Jr.**: column 13, lines 50-54).

In regard to claim 18, **Breternitz, Jr.** disclosed the limitations:

- *A computer-implemented method comprising:*
  - *selecting a representative path within an inner region of a software function, the representative path being identified by a single entry node, and a single representative exit node* (column 13, lines 32-54 and column 14, lines 7-35);

Breternitz, Jr. did not explicitly state *selecting a single one of the existing entry nodes as a representative entry node for the inner region* and *replacing the inner region with the representative entry node*. **Tenev** demonstrated that it was known at the time of invention to construct graphs such that one node is selected as a representative of other nodes (Figure 9; element 510 and 514) and replacing the other nodes with the single node (Figure 9, elements 520, 522 and 524). It would have been obvious to one of ordinary skill in the art at the time of invention to implement **Breternitz, Jr.**'s single entry single exit control flow graph system with one selected node as representative of other nodes as found in **Tenev**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide more information in a single graph (for example, this aids in expansion and contraction of nodes, column 3, liens 25-34); additionally, along this same line of reasoning, the implementation would have been obvious because of ordinary skill in the art would be motivated to provide the compiler optimizations to a greater amount of code, which would be represented with a compact CFG containing global information.

Neither **Breternitz, Jr.** nor **Tenev** did not explicitly state inner region with multiple entry and exit nodes; *for each prolog node of the inner region having an edge to one of the existing entry nodes that is not the representative entry node, adding an edge from the prolog node to the representative entry node; and for each epilog node of the inner region having an edge to one of the existing exit nodes that is not the representative exit node, adding an edge from the representative exit node to the epilog node.* **Bharadwaj** demonstrated that it was known at the time of invention to provide control flow regions with multiple entry and exit points (column 4, line 61 to column 5, line 14), which implies multiple prolog nodes with an edge other than the "representative" entry node and epilog nodes to match exit nodes as well (remembering super/extended basic blocks have multiple exits to other nodes and reverse super/extended basic blocks have multiple entries from other nodes). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the single entry single exit CFG of **Breternitz, Jr** and **Tenev** with CFG's having multiple entry nodes and with adding an edge between entry/exit and prolog/epilog nodes respectively as suggested by **Bharadwaj**'s teaching and **Breternitz, Jr.**'s own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implementing standard CFG situations (multiple prolog and epilog nodes) with the benefits of single entry single exit (**Breternitz, Jr.**: column 13, lines 50-54).

In regard to claim 19, the rejection of claim 18 is incorporated herein and further **Breternitz, Jr.**, **Tenev** and **Bharadwaj** did not explicitly state the limitations: *removing*

any edges from prolog nodes of the inner region to entry nodes of the inner region other than the representative entry node; and removing any edges from exit nodes of the inner region other than the representative exit node to epilog nodes of the inner region. However, **Breternitz, Jr.** did disclose the benefits of single entry single exit CFGs for analysis of compilations (column 13, lines 50-54) and indicated the need to transform CFGs to the SESE in regions and blocks for program optimization (column 13, lines 50-54). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the single entry single exit CFG of **Breternitz, Jr** and **Tenev** with removing edges between entry/exit and prolog/epilog nodes respectively as suggested by **Breternitz, Jr.**'s own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to implementing standard CFG situations (multiple prolog and epilog nodes) with the benefits of single entry single exit (**Breternitz, Jr.**: column 13, lines 50-54 and for above reasoning under claim 18).

In regard to claim 20, **Breternitz, Jr.**, **Tenev** and **Bharadwaj** did not explicitly state the limitations: *wherein the software function has a function entry and a function exit, and the inner region has at least one entry node and at least one exit node, the method further comprising: adding an edge from the function entry to each of the at least one entry node of the inner region; and adding an edge from each of the at least one exit node of the inner region to the function exit.* However, **Breternitz, Jr.** demonstrated that it was known at the time of invention to utilize nested single-entry-single exit regions within code (column 13, lines 50-54 and column 14, lines 7-10). It would have

been obvious to one of ordinary skill in the art at the time of invention to implement the SESE CFG system of **Breternitz, Jr.**, **Tenev** and **Bharadwaj** with adding an edge between a function entry/exit and the inner region entry/exit respectively as suggested by **Breternitz, Jr.**'s own teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to correctly connect the nested regions once the CFG is formed, which could easily consist of one function that contains only two inner regions of the same level, thus requiring them to be directly connected to the function entry/exit.

In regard to claim 21, **Breternitz, Jr.**, **Tenev** and **Bharadwaj** further disclosed the limitation *wherein the control flow graph includes a plurality of inner regions, and the actions of the method are applied for each of the plurality of inner regions* (**Breternitz, Jr.**: column 13, lines 50-54).

In regard to claim 22, **Breternitz, Jr.**, **Tenev** and **Bharadwaj** further disclosed the limitation *wherein the control flow graph includes a hierarchy of inner regions, and the actions of the method are applied recursively to the hierarchy of inner regions* (**Breternitz, Jr.**: column 13, lines 50-54; column 14, lines 7-10).

In regard to claim 24, **Breternitz, Jr.**, **Tenev** and **Bharadwaj** disclosed the limitations claim 18, which correspond to the limitations of the current claim, as such the rejection of claim 18 is incorporated herein as the rejection of the current claim.

In regard to claims 25, the limitations of the claim correspond to the limitations of claim 20 and as such claim 20's rejection is incorporated and applied here as well.

12. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Breternitz, Jr.** et al. (USPN 6,381,739) in view of **Tenev** et al. (USPN 6,108,698) in further view of **Bharadwaj** (USPN 5,894,576) as applied to claim 13 and in further view of "Advanced Compiler Design Implementation" by Steve S. **Muchnick**.

In regard to claim 15, **Breternitz, Jr.**, **Tenev** and **Bharadwaj** did not explicitly state the limitations:

- *creating a region source node for the outer region;*
- *for each entry node of the outer region, adding an edge from the region source node to the entry node;*
- *creating a region sink node for the outer region; and*
- *for each exit node of the outer region, adding an edge from the exit node to the region sink node.*

Muchnick demonstrated that it was known at the time of invention to adding source and sink nodes and adding edges between the source/sink nodes and the entry/exit nodes respectively (page 171, first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to implement the single entry single exit CFG system **Breternitz, Jr.**, **Tenev** and **Bharadwaj** with source and sink nodes as described

above by **Muchnick**'s teaching. This implementation would have been obvious because one of ordinary skill in the art would be motivated to utilize well-known techniques for analysis and optimization of code (page 171, first paragraph; page 174, last paragraph).

In regard to claim 16, **Breternitz, Jr.**, **Tenev**, **Bharadwaj** and **Muchnick** disclosed the limitation *wherein the control flow graph includes a plurality of inner regions, and the actions of the method are applied for each of the plurality of inner regions, such that a different augmented control flow graph is created for each of the plurality of inner regions* (**Breternitz, Jr.**: column 13, lines 50-54).

In regard to claim 17, **Breternitz, Jr.**, **Tenev**, **Bharadwaj** and **Muchnick** disclosed the limitation *wherein the control flow graph includes a hierarchy of inner regions, and the actions of the method are applied recursively to the hierarchy of inner regions, such that a different augmented control flow graph is created for each inner region in the hierarchy of inner regions* (**Breternitz, Jr.**: column 13, lines 50-54; column 14, lines 7-10).

Allowable Subject Matter

13. Claims 14 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: claims 14 and 23 contain the limitations *assigning edge values to all edges in the control flow graph such that the sum of the edge values along each unique path unique within the control flow graph*, which the prior art of record does not fairly suggest in combination or motivate to combine with the limitations of the dependent claims.

Response to Arguments

15. Applicant's arguments with respect to claims 13-25 and 40-67 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
September 4, 2003

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